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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CUTLER, ALBERT H	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/679,727	LI ET AL.	
	Examiner	Art Unit	
	Albert H. Cutler	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *23-42,45 and 46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *23-42, 45 and 46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is responsive to communication filed on May 31, 2007. Claims 23-42, 45, and 46 are pending in the application and have been examined by the Examiner.

Response to Arguments

2. Applicant's arguments with respect to claims 23-42 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 23-25, 29-34, and 38-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rumbaugh(US 6,449,318) in view of Bechtel et al.(US 5,990,469).

Consider claim 23, Rumbaugh teaches:

A host processor to camera interface(figure 2, column 4, line 10 through column 5, line 60), comprising:

a camera side interface("Transmitter", see top half of figure 2, the camera side interface can be used to connect a camera, digital video device, etc., column 4, lines 12-30), including:

a camera side link layer("Electronic Device Interface", 100, figure 2) coupled to a

camera(column 4, lines 12-30), the camera providing video data(column 4, line 16), the camera side link layer(100) converting the video data to a desired video data format(The camera side link layer converts the input signal into bits(i.e. a desired video data format) which are read into a serial interface, column 4, lines 31-33.);

a serializer("Serial Interface", 101, figure 2) coupled to the camera side link layer(see figure 2) for serializing the video data in the desired video data format(column 4, lines 31-45); and

a camera side transmitter("transceiver", 102, figure 2) coupled to the serializer(see figure 2), the camera side transmitter(102) transmitting the serialized video data(column 4, line 46 through column 5, line 9);

a host processor side interface("Receiver", bottom half of figure 2), including:

a host processor side receiver(The host processor side receiver is comprised of a decoupler(i.e. receiver, 107) which properly receives the transmitted data, column 5, lines 12-19.) for receiving the serialized video data(The decoupler is connected to the twisted pair wiring which carries the incoming serialized data, column 5, lines 12-15);

a deserializer("serial interface buffer", 111, figure 2) coupled to the host processor side receiver(see figure 2, the deserializer(111) is coupled through 108, 109, and 110 to the receiver(107)), the deserializer deserializing the serialized video data(The deserializer provides a converter(i.e. converts the serial data to parallel data) or a serial bit stream, figure 2, 111.);

and a host processor side link layer("Electronic Device Interface", 112, figure 2) coupled to the deserializer(111) and a host processor(The host processor link

layer("digital data interface input device", 112, column 5, lines 34-36) can be used to connect to a computer(i.e. a host processor), column 5, lines 34-36), wherein the host processor side link layer(112) is adapted to convert the deserialized video data into a format compatible with the host processor when required(The host processor side link layer(112) interfaces with a computer(column 5, lines 34-36), and thus inherently converts the video data into a compatible format, as an interface is defined as an arrangement of equipment or programs designed to communicate information from one system of computing devices or programs to another, and enabling separate and sometimes incompatible elements to coordinate effectively.); and

a cable("Twisted Pair Wiring", figure 2) for carrying the video data(column 4, lines 1-9), the cable including a pair of power wires(The cable is a twisted pair copper wire(i.e. a pair of power wires)) for carrying power(column 4, lines 1-9), the cable coupling the camera side transmitter to the host processor side receiver(see figure 2, column 4, line 65 through column 5, line 15).

However, Rumbaugh only teaches of a pair of power wires for transmitting a data signal(column 4, lines 1-9), and does not explicitly teach of a data signal line as well as a pair of power wires. Furthermore, Rumbaugh does not explicitly teach that the host processor side link layer provides a trigger pulse to the camera side link layer through the pair of power wires which is indicative of initiation of configuration of the camera, wherein data communication from the camera to the host processor is disabled and configuration data is transmitted from the host processor to the camera during the configuration, and following the configuration of the camera, communication from the

camera to the host processor is enable and video data is transmitted from the camera to the host processor via the data signal line.

Bechtel et al. are similar to Rumbaugh in that Betchtel et al. teach of a camera(106, figure 5, 1-4, figure 9) which transmits data to a processor(204, figure 5, 5 figure 9). See column 4, lines 19-44, column 8, lines 36-54.

However, in addition to the teachings of Rumbaugh, Bechtel et al. teach of separate pins for power and for transmitting data(see column 4, lines 38-44). Bechtel et al. teach that three pins are used for a serial interface(i.e. as a data signal line) between the microcontroller and the camera. Bechtel et al. also teach of a ground pin and a V+ supply pin(i.e. a pair of power wires). In column 23, line 46 through column 24, line 33, Bechtel et al. detail the serial peripheral interface (SPI) between the camera portion(ASIC XC4003E) and the processor(microcontroller(5)). Bechtel et al. teach that in the SPI there are three bi-directional lines for transmitting data and a slave select input (SS) which includes a ground(i.e. is a pair of power wires), the slave select input being operable to change the states of the camera and microcontroller alternately between master and slave.

Additionally, Bechtel et al. teach of providing a trigger pulse to the camera side through the pair of power wires which is indicative of initiation of configuration of the camera(The slave select signal, which is provided by a pair of power wires as illustrated above, is driven to line low(i.e. provided a trigger pulse), which places the ASIC XC4003E(i.e. the camera side) in a slave state, column 24, lines 1-5.), wherein data communication from the camera to the host processor is disabled(The camera is placed

in slave mode(i.e. communication from the camera to the host processor is disabled), column 24, lines 1-5.) and configuration data is transmitted(A nine byte instruction is transmitted, column 24, lines 5-6) from the host processor to the camera during the configuration(column 24, lines 1-6), and following the configuration of the camera, communication from the camera to the host processor is enabled and video data is transmitted from the camera to the host processor via the data signal line(See column 24, lines 16-23. After the instruction(i.e. configuration) is received, the camera side is set to the master and the microcontroller side is set to the slave, enabling pixel data(i.e. video data) to be transmitted over the data signal line.).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to use a bidirectional bus with a data signal line and a pair of power wires as taught by Bechtel et al. in place of the pair of wires taught by Rumbaugh, and to provide configuration data from the host processor side to the camera side as taught by Bechtel et al. for the benefit of creating a control system which is able to efficiently control various aspects of the image array sensor, such as windowing, mode of operation, sensitivity as well as other parameters in order to reduce the data throughout(Bechtel et al., column 3, lines 26-33).

Consider claim 24, and as applied to claim 23 above, Rumbaugh further teaches that the camera side link layer(100) is configured to convert a plurality of camera video data formats into the desired video format(The electronic device interface(i.e. camera side link layer) interfaces with a multitude of electronic devices(i.e. a plurality of data

formats), some of which provide video data(column 4, lines 16-30), and converts these data formats into bits(i.e. the desired video format) that are read into the serializer, column 4, lines 31-33.).

Consider claim 25, and as applied to claim 24 above, Rumbaugh teaches that the camera side interface receives a plurality of camera video data formats and converts said video data formats into the desired video format(see claim 24 rationale). Rumbaugh further teaches that a serial interface converter(101) may be necessary when parallel transmission methods are involved, column 4, lines 33-35. Parallel transmission methods mean that a multitude of parallel transmission lines can be used to transmit bits. The combination of Rumbaugh and Bechtel et al. does not explicitly teach that the camera video data formats include a single 8-bit data format, a dual 8-bit data format, a single 16-bit data format, a single 24-bit data format and a single 12-bit data format.

However, **Official Notice** (MPEP § 2144.03) is taken that both the concepts and advantages of having an interface compatible with multiple video data input formats such as a single 8-bit data format, a dual 8-bit data format, a single 16-bit data format, a single 24-bit data format and a single 12-bit data format are well known and expected in the art. It would have been obvious to a person having ordinary skill in the art at the time of the invention to include an input interface that is compatible with a single 8-bit data format, a dual 8-bit data format, a single 16-bit data format, a single 24-bit data format and a single 12-bit data format into the device taught by the combination of

Rumbaugh and Bechtel et al. for the benefit of providing a data transmission medium with improved versatility, compatibility, and marketability by accepting multiple bus sizes which transmit many well known video data formats.

It should be noted that the common knowledge for having an interface compatible with multiple video data input formats such as a single 8-bit data format, a dual 8-bit data format, a single 16-bit data format, a single 24-bit data format and a single 12-bit data format **is taken as admitted prior art** because Applicant failed to seasonably traverse this common knowledge from the amendment filed on May 31, 2007. See MPEP § 2144.03. In re Chevenard, 60 USPQ 239 (CCPA 1943).

Consider claim 29, and as applied to claim 23 above, Rumbaugh et al. further teach that the functionality of the host processor side link layer(112) is incorporated within the host processor(The serial interface buffer(111) can be connected directly to a computer(i.e. a host processor) instead of going through a digital data interface(i.e. a link layer), column 5, lines 34-36.).

Consider claim 30, and as applied to claim 23 above, Rumbaugh teaches a low-voltage differential signaling (LVDS) receiver for serial-to-camera channel communications located within the camera side interface(Rumbaugh teaches of a transceiver(102) located within the camera side interface(see figure 2, column 4, lines 38-49). Rumbaugh teaches that various devices can use the electronic device interface, including low voltage differential signaling(LVDS) devices, column 4, lines 12-

26. Therefore, if the interfacing device is an LVDS device, then the receiver must be an LVDS receiver. Also communication between the camera and host processor is done using a serial interface(i.e. a serial-to-camera channel, column 4, lines 31-45)). Rumbaugh further teaches that an output of the LVDS receiver is coupled to the camera side link layer(see figure 2, the LVDS receiver(102) is coupled to the camera side link layer(100) through the signaling interface(101)).

Bechtel et al. teach of a bidirectional interface capable of reconfiguring a camera via a host processor, and sending images to a host processor via a camera(column 23, line 46 through column 24, line 34, claim 23 rationale).

Furthermore, Bechtel et al. teach that inputs of the receiver are coupled to outputs of the camera side transmitter(See column 23, lines 46 through column 24, line 34. As the bus is bidirectional, the outputs of the camera side transmitter are the same as the inputs of the camera side receiver.); and

A transmitter for SERTC channel communications located within the host processor side interface, wherein an input of the LVDS transmitter is coupled to the host processor side link layer and outputs of the LVDS transmitter are coupled to inputs of the host processor side receiver(See column 23, lines 46 through column 24, line 34. As the bus is bidirectional, the outputs of the host processor side transmitter(i.e. the microcontroller, 5) are the same as the inputs of the host processor side receiver.).

Bechtel et al. do not explicitly teach that the transmitters are respectively connected to host processor and camera side link layers. However, because Rumbaugh teaches of host processor and camera side link layers, the combination of

Rumbaugh and Bechtel et al. teaches that the transmitters are respectively connected to host processor and camera side link layers.

Consider claim 31, and as applied to claim 30 above, Rumbaugh further teaches that the cable includes a first pair of signal wires for carrying the video data(The cable is a twisted pair(i.e. a first pair of signal wires), column 4, lines 1-9, figure 2. The cable is used for carrying video data, column 4, lines 14-30.), and wherein the video data is in the form of a low-voltage differential signaling (LVDS) data stream(The interfaced device may be a LVDS device(i.e. a device which transmits LVDS data) column 4, line 26).

Bechtel et al. also teach of at least a pair of signal wires used to carry video data(Three pins are used for data transfer, see claim 23 rationale.).

Consider claim 32, and as applied to claim 31 above, Rumbaugh teaches of a camera side link layer, and a host processor side link layer(see claim 23 rationale). Rumbaugh also teaches of a first pair of wires which communicate video data in the desired format(see claim 31 rationale).

However, Rumbaugh does not explicitly teach that the camera side link layer and the host processor side link layer are configured to share the first pair of signal wires to communicate the video data in the desired video signal format and configuration signals for the SERTC channel.

However, Bechtel et al. teach that the signal wires are shared to communicate

video signals and configuration signals(The bus is bi-directional, see column 23, line 46 through column 24, line 34, claim 23 rationale.).

Consider claim 33, and as applied to claim 30 above, Rumbaugh does not explicitly teach that the cable further includes a second pair of signal wires to communicate configuration signals for the SERTC channel.

However, Bechtel et al. teaches that the cable further includes a second pair of signal wires to communicate configuration signals for the SERTC channel(A second pair of signal wires, including V+ and ground, are used to switch between master and slave settings(i.e. communicate configuration signals), see claim 23 rationale, column 23, line 46 through column 24, line 34.).

Consider claim 34, Rumbaugh teaches:

A host processor to camera interface(figure 2, column 4, line 10 through column 5, line 60), comprising:

a camera side interface("Transmitter", see top half of figure 2, the camera side interface can be used to connect a camera, digital video device, etc., column 4, lines 12-30), including:

a camera side link layer("Electronic Device Interface", 100, figure 2) coupled to a camera(column 4, lines 12-30), the camera providing video data(column 4, line 16), the camera side link layer(100) converting the video data to a desired video data format(The camera side link layer converts the input signal into bits(i.e. a desired video

data format) which are read into a serial interface, column 4, lines 31-33.);

a serializer("Serial Interface", 101, figure 2) coupled to the camera side link layer(see figure 2) for serializing the video data in the desired video data format(column 4, lines 31-45); and

a camera side transmitter("transceiver", 102, figure 2) coupled to the serializer(see figure 2), the camera side transmitter(102) transmitting the serialized video data(column 4, line 46 through column 5, line 9);

a host processor side interface("Receiver", bottom half of figure 2), including:

a host processor side receiver(The host processor side receiver is comprised of a decoupler(i.e. receiver, 107) which properly receives the transmitted data, column 5, lines 12-19.) for receiving the serialized video data(The decoupler is connected to the twisted pair wiring which carries the incoming serialized data, column 5, lines 12-15);

a deserializer("serial interface buffer", 111, figure 2) coupled to the host processor side receiver(see figure 2, the deserializer(111) is coupled through 108, 109, and 110 to the receiver(107)), the deserializer deserializing the serialized video data(The deserializer provides a converter(i.e. converts the serial data to parallel data) or a serial bit stream, figure 2, 111.);

and a host processor side link layer("Electronic Device Interface", 112, figure 2) coupled to the deserializer(111) and a host processor(The host processor link layer("digital data interface input device", 112, column 5, lines 34-36)) can be used to connect to a computer(i.e. a host processor), column 5, lines 34-36), wherein the host processor side link layer(112) is adapted to convert the deserialized video data into a

format compatible with the host processor when required(The host processor side link layer(112) interfaces with a computer(column 5, lines 34-36), and thus inherently converts the video data into a compatible format, as an interface is defined as an arrangement of equipment or programs designed to communicate information from one system of computing devices or programs to another, and enabling separate and sometimes incompatible elements to coordinate effectively.); and

a cable("Twisted Pair Wiring", figure 2) for carrying the video data(column 4, lines 1-9), the cable including a pair of power wires(The cable is a twisted pair copper wire(i.e. a pair of power wires)) for carrying power(column 4, lines 1-9), the cable coupling the camera side transmitter to the host processor side receiver(see figure 2, column 4, line 65 through column 5, line 15).

However, Rumbaugh only teaches of a pair of power wires for transmitting a data signal(column 4, lines 1-9), and does not explicitly teach of a data signal line as well as a pair of power wires. Furthermore, Rumbaugh does not explicitly teach that the host processor side link layer provides a trigger pulse to the camera side link layer through the pair of power wires which is indicative of initiation of configuration of the camera, wherein data communication from the camera to the host processor is disabled and configuration data is transmitted from the host processor to the camera during the configuration, and following the configuration of the camera, communication from the camera to the host processor is enable and video data is transmitted from the camera to the host processor via the data signal line. Also, although Rumbaugh teaches of a camera remote from a processor, Rumbaugh does not explicitly teach that the camera

is attached to a motor vehicle, or that the host processor is incorporated within an electronic control unit of the motor vehicle.

Rumbaugh also does not teach that the camera side link layer is configured to convert a plurality of camera video data formats into the desired video data format, and wherein the camera video data formats include a single 8-bit data format, a dual 8-bit data format, a single 16-bit data format, a single 24-bit data format and a single 12-bit data format.

Bechtel et al. are similar to Rumbaugh in that Betchtel et al. teach of a camera(106, figure 5, 1-4, figure 9) which transmits data to a processor(204, figure 5, 5 figure 9). See column 4, lines 19-44, column 8, lines 36-54.

However, in addition to the teachings of Rumbaugh, Bechtel et al. teach of separate pins for power and for transmitting data(see column 4, lines 38-44). Bechtel et al. teach that three pins are used for a serial interface(i.e. as a data signal line) between the microcontroller and the camera. Bechtel et al. also teach of a ground pin and a V+ supply pin(i.e. a pair of power wires). In column 23, line 46 through column 24, line 33, Bechtel et al. detail the serial peripheral interface (SPI) between the camera portion(ASIC XC4003E) and the processor(microcontroller(5)). Bechtel et al. teach that in the SPI there are three bi-directional lines for transmitting data and a slave select input (SS) which includes a ground(i.e. is a pair of power wires), the slave select input being operable to change the states of the camera and microcontroller alternately between master and slave.

Additionally, Bechtel et al. teach of providing a trigger pulse to the camera side

through the pair of power wires which is indicative of initiation of configuration of the camera(The slave select signal, which is provided by a pair of power wires as illustrated above, is driven to line low(i.e. provided a trigger pulse), which places the ASIC XC4003E(i.e. the camera side) in a slave state, column 24, lines 1-5.), wherein data communication from the camera to the host processor is disabled(The camera is placed in slave mode(i.e. communication from the camera to the host processor is disabled), column 24, lines 1-5.) and configuration data is transmitted(A nine byte instruction is transmitted, column 24, lines 5-6) from the host processor to the camera during the configuration(column 24, lines 1-6), and following the configuration of the camera, communication from the camera to the host processor is enabled and video data is transmitted from the camera to the host processor via the data signal line(See column 24, lines 16-23. After the instruction(i.e. configuration) is received, the camera side is set to the master and the microcontroller side is set to the slave, enabling pixel data(i.e. video data) to be transmitted over the data signal line.). Bechtel further teach that the camera is attached to a motor vehicle(See figure 1, figure 5, columns 4-8), and that the host processor(204, figure 5) is incorporated within an electronic control unit of the motor vehicle(See figure 5, the host processor(204) is incorporated within a control unit(205) for controlling the headlamps(206) of a motor vehicle.).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to use a bidirectional bus with a data signal line and a pair of power wires as taught by Bechtel et al. in place of the pair of wires taught by Rumbaugh, and to provide configuration data from the host processor side to the

camera side as taught by Bechtel et al. for the benefit of creating a control system which is able to efficiently control various aspects of the image array sensor, such as windowing, mode of operation, sensitivity as well as other parameters in order to reduce the data throughout(Bechtel et al., column 3, lines 26-33).

The combination of Rumbaugh and Bechtel et al. teaches of a camera and host processor system incorporated in a motor vehicle. However, the combination does not explicitly teach that the camera side link layer is configured to convert a plurality of camera video data formats into the desired video data format, and wherein the camera video data formats include a single 8-bit data format, a dual 8-bit data format, a single 16-bit data format, a single 24-bit data format and a single 12-bit data format.

However, **Official Notice** (MPEP § 2144.03) is taken that both the concepts and advantages of having an interface compatible with multiple video data input formats such as a single 8-bit data format, a dual 8-bit data format, a single 16-bit data format, a single 24-bit data format and a single 12-bit data format are well known and expected in the art. It would have been obvious to a person having ordinary skill in the art at the time of the invention to include an input interface that is compatible with a single 8-bit data format, a dual 8-bit data format, a single 16-bit data format, a single 24-bit data format and a single 12-bit data format into the device taught by the combination of Rumbaugh and Bechtel et al. for the benefit of providing a data transmission medium with improved versatility, compatibility, and marketability by accepting multiple bus sizes which transmit many well known video data formats.

It should be noted that the common knowledge for having an interface compatible with multiple video data input formats such as a single 8-bit data format, a dual 8-bit data format, a single 16-bit data format, a single 24-bit data format and a single 12-bit data format **is taken as admitted prior art** because Applicant failed to seasonably traverse this common knowledge from the amendment filed on May 31, 2007. See MPEP § 2144.03. In re Chevenard, 60 USPQ 239 (CCPA 1943).

Consider claim 38, and as applied to claim 34 above, Rumbaugh et al. further teach that the functionality of the host processor side link layer(112) is incorporated within the host processor(The serial interface buffer(111) can be connected directly to a computer(i.e. a host processor) instead of going through a digital data interface(i.e. a link layer), column 5, lines 34-36.).

Consider claim 39, and as applied to claim 34 above, Rumbaugh teaches a low-voltage differential signaling (LVDS) receiver for serial-to-camera channel communications located within the camera side interface(Rumbaugh teaches of a transceiver(102) located within the camera side interface(see figure 2, column 4, lines 38-49). Rumbaugh teaches that various devices can use the electronic device interface, including low voltage differential signaling(LVDS) devices, column 4, lines 12-26. Therefore, if the interfacing device is an LVDS device, then the receiver must be an LVDS receiver. Also communication between the camera and host processor is done using a serial interface(i.e. a serial-to-camera channel, column 4, lines 31-45)).

Rumbaugh further teaches that an output of the LVDS receiver is coupled to the camera side link layer(see figure 2, the LVDS receiver(102) is coupled to the camera side link layer(100) through the signaling interface(101)).

Bechtel et al. teach of a bidirectional interface capable of reconfiguring a camera via a host processor, and sending images to a host processor via a camera(column 23, line 46 through column 24, line 34, claim 34 rationale).

Furthermore, Bechtel et al. teach that inputs of the receiver are coupled to outputs of the camera side transmitter(See column 23, lines 46 through column 24, line 34. As the bus is bidirectional, the outputs of the camera side transmitter are the same as the inputs of the camera side receiver.); and

A transmitter for SERTC channel communications located within the host processor side interface, wherein an input of the LVDS transmitter is coupled to the host processor side link layer and outputs of the LVDS transmitter are coupled to inputs of the host processor side receiver(See column 23, lines 46 through column 24, line 34. As the bus is bidirectional, the outputs of the host processor side transmitter(i.e. the microcontroller, 5) are the same as the inputs of the host processor side receiver.).

Bechtel et al. do not explicitly teach that the transmitters are respectively connected to host processor and camera side link layers. However, because Rumbaugh teaches of host processor and camera side link layers, the combination of Rumbaugh and Bechtel et al. teaches that the transmitters are respectively connected to host processor and camera side link layers.

Consider claim 40, and as applied to claim 39 above, Rumbaugh further teaches that the cable includes a first pair of signal wires for carrying the video data(The cable is a twisted pair(i.e. a first pair of signal wires), column 4, lines 1-9, figure 2. The cable is used for carrying video data, column 4, lines 14-30.), and wherein the video data is in the form of a low-voltage differential signaling (LVDS) data stream(The interfaced device may be a LVDS device(i.e. a device which transmits LVDS data) column 4, line 26).

Bechtel et al. also teach of at least a pair of signal wires used to carry video data(Three pins are used for data transfer, see claim 34 rationale.)

Consider claim 41, and as applied to claim 40 above, Rumbaugh teaches of a camera side link layer, and a host processor side link layer(see claim 23 rationale). Rumbaugh also teaches of a first pair of wires which communicate video data in the desired format(see claim 31 rationale).

However, Rumbaugh does not explicitly teach that the camera side link layer and the host processor side link layer are configured to share the first pair of signal wires to communicate the video data in the desired video signal format and configuration signals for the SERTC channel.

However, Bechtel et al. teach that the signal wires are shared to communicate video signals and configuration signals(The bus is bi-directional, see column 23, line 46 through column 24, line 34, claim 34 rationale.).

Consider claim 42, and as applied to claim 40 above, Rumbaugh does not explicitly teach that the cable further includes a second pair of signal wires to communicate configuration signals for the SERTC channel.

However, Bechtel et al. teaches that the cable further includes a second pair of signal wires to communicate configuration signals for the SERTC channel(A second pair of signal wires, including V+ and ground, are used to switch between master and slave settings(i.e. communicate configuration signals), see claim 34 rationale, column 23, line 46 through column 24, line 34.).

5. Claims 26-28, and 35-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rumbaugh in view of Bechtel et al. as applied to claim 34 above, and further in view of Beiley et al.(U.S. Patent 6,522,357), and further in view of Michael(U.S. Patent 4,025,947).

Consider claim 26, and as applied to claim 24 above, Rumbaugh teaches of transmitting video data(see claim 23 rationale) and timing information(column 5, lines 38-61), and of a link layer(see claim 23 rationale).

However, the combination of Rumbaugh and Bechtel et al. does not explicitly teach that at least one of the camera video data formats provides a frame valid (FVAL) signal and a line valid (LVAL) signal, and wherein the camera side link layer combines the FVAL signal and the LVAL signal into a single validation (XVAL) signal.

Beiley is similar to Rumbaugh in that an image sensor(408, figure 4) is used to

capture an image, and the image sensor communicates serially with a host processor(column 5, lines 49-52).

In addition to the teachings of Rumbaugh and Bechtel et al., Beiley et al. teach at least one of the camera video data formats provides a frame valid (FVAL) signal and a line valid (LVAL) signal(A frame valid signal is used to indicate valid data for a frame, and a line valid signal is inserted at the start of every row, Column 5, lines 53-60.).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to have at least one of the camera video data formats provide a frame valid (FVAL) signal and a line valid (LVAL) signal as taught by Beiley et al. in the data transmission medium taught by the combination of Rumbaugh and Bechtel et al. in order to indicate valid data(column 5, lines 53-60) and thus prevent a data loss and discrepancies between an original frame captured by the image sensor and a frame reconstructed by the host processor.

The combination of Rumbaugh, Bechtel et al., and Beiley et al. teaches of providing timing information, and of a frame valid signal and a line valid signal.

However, the combination of Rumbaugh, Bechtel et al. and Beiley et al. does not explicitly teach that the FVAL signal and the LVAL signal are combined into a single validation (XVAL) signal.

Michael is similar to Rumbaugh in that Michael is concerned with transmission of video data(column 3, lines 13-33). Michael is also similar in that a serializer(13, figure 3), and a deserializer(18, figure 3) are used to convert parallel data into serial data for transmission, and serial data into parallel data upon the reception of said

transmission(column 3, lines 26-55).

However, in addition to the teachings of Rumbaugh, Bechtel et al. and Beiley et al., Michael teaches of combining multiple signals into a single validation signal(see figure 9, column 6, lines 15-30). In figure 9, under the label "General", Michael teaches a signal envelope indicated by a rectangle with diagonal lines, said envelope contained within a beginning "start" pulse, and an ending "Stop" pulse. Michael further teaches, under the label "Sync", that a synchronization signal is provided parallel to the signal envelope to provide the "start and "stop" pulses. In addition to this, Michael teaches that the signal envelope, and the bit data encloses within it, can be combined with the "Sync" signal to produce one all-encompassing signal containing both bit-data and timing information(see bottom of figure 9, column 5, line 65 through column 6, line 30).

The signal envelope of Michael is analogous to the frame valid signal of Beiley et al. in that it represents a period in which valid data is contained. That valid data is bit data, as is shown in the bottom of figure 9, and that bit data is analogous to the line valid data of Beiley et al. Therefore, the data pattern shown at the bottom of figure 9, and explained in column 6, lines 15-30, represents a single validation signal which contains a signal envelope(analogous to a the frame valid signal) and a bitstream(analogous to a line valid signal).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to combine the frame valid signal and line valid signal taught by the combination of Rumbaugh, Bechtel et al. and Beiley et al. into one single validation signal as taught by Michael because a single validation signal is the simplest

type of signal, and it has the advantage that no synchronization information is required as each piece of data is fully self contained(Michael, column 6, line 23-30).

Consider claim 27, and as applied to claim 26 above, Rumbaugh, Bechtel et al., and Beiley et al. do not explicitly teach that the XVAL signal corresponds to the LVAL signal with and added EOF signal.

However, Michael teaches that the XVAL signal corresponds to the LVAL signal(see figure 9, claim 26 rationale) with and added EOF signal("stop pulse", figure 9, column 6, lines 5-14).

Consider claim 28, and as applied to claim 27 above, Rumbaugh, Bechtel et al., and Beiley et al. do not explicitly teach that a pulse width of the EOF signal is less than the pulse width of the LVAL signal.

However, Michael teaches that a pulse width of the EOF signal is less than the pulse width of the LVAL signal(The LVAL signal taught by Beiley et al. has to be wide enough to indicate the validity of an entire line of data which is composed of a large number of bits. The EOF signal taught by Michael is only one bit long as the signal of Michael comprises a start bit, eight data bits, and a stop bit(i.e. EOF signal, column 6, lines 18-30, see figure 9).

Consider claim 35, and as applied to claim 34 above, Rumbaugh teaches of transmitting video data(see claim 34 rationale) and timing information(column 5, lines

38-61), and of a link layer(see claim 34 rationale).

However, the combination of Rumbaugh and Bechtel et al. does not explicitly teach that at least one of the camera video data formats provides a frame valid (FVAL) signal and a line valid (LVAL) signal, and wherein the camera side link layer combines the FVAL signal and the LVAL signal into a single validation (XVAL) signal.

Beiley is similar to Rumbaugh in that an image sensor(408, figure 4) is used to capture an image, and the image sensor communicates serially with a host processor(column 5, lines 49-52).

In addition to the teachings of Rumbaugh and Bechtel et al., Beiley et al. teach at least one of the camera video data formats provides a frame valid (FVAL) signal and a line valid (LVAL) signal(A frame valid signal is used to indicate valid data for a frame, and a line valid signal is inserted at the start of every row, Column 5, lines 53-60.).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to have at least one of the camera video data formats provide a frame valid (FVAL) signal and a line valid (LVAL) signal as taught by Beiley et al. in the data transmission medium taught by the combination of Rumbaugh and Bechtel et al. in order to indicate valid data(column 5, lines 53-60) and thus prevent a data loss and discrepancies between an original frame captured by the image sensor and a frame reconstructed by the host processor.

The combination of Rumbaugh, Bechtel et al., and Beiley et al. teaches of providing timing information, and of a frame valid signal and a line valid signal.

However, the combination of Rumbaugh, Bechtel et al., and Beiley et al. does not

explicitly teach that the FVAL signal and the LVAL signal are combined into a single validation (XVAL) signal.

Michael is similar to Rumbaugh in that Michael is concerned with transmission of video data(column 3, lines 13-33). Michael is also similar in that a serializer(13, figure 3), and a deserializer(18, figure 3) are used to convert parallel data into serial data for transmission, and serial data into parallel data upon the reception of said transmission(column 3, lines 26-55).

However, in addition to the teachings of Rumbaugh, Bechtel et al., and Beiley et al., Michael teaches of combining multiple signals into a single validation signal(see figure 9, column 6, lines 15-30). In figure 9, under the label "General", Michael teaches a signal envelope indicated by a rectangle with diagonal lines, said envelope contained within a beginning "start" pulse, and an ending "Stop" pulse. Michael further teaches, under the label "Sync", that a synchronization signal is provided parallel to the signal envelope to provide the "start and "stop" pulses. In addition to this, Michael teaches that the signal envelope, and the bit data encloses within it, can be combined with the "Sync" signal to produce one all-encompassing signal containing both bit-data and timing information(see bottom of figure 9, column 5, line 65 through column 6, line 30).

The signal envelope of Michael is analogous to the frame valid signal of Beiley et al. in that it represents a period in which valid data is contained. That valid data is bit data, as is shown in the bottom of figure 9, and that bit data is analogous to the line valid data of Beiley et al. Therefore, the data pattern shown at the bottom of figure 9, and explained in column 6, lines 15-30, represents a single validation signal which

contains a signal envelope(analogous to a the frame valid signal) and a bitstream(analogous to a line valid signal).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to combine the frame valid signal and line valid signal taught by the combination of Rumbaugh, Bechtel et al., and Beiley et al. into one single validation signal as taught by Michael because a single validation signal is the simplest type of signal, and it has the advantage that no synchronization information is required as each piece of data is fully self contained(Michael, column 6, line 23-30).

Consider claim 36, and as applied to claim 35 above, Rumbaugh, Bechtel et al., and Beiley et al. do not explicitly teach that the XVAL signal corresponds to the LVAL signal with and added EOF signal.

However, Michael teaches that the XVAL signal corresponds to the LVAL signal(see figure 9, claim 35 rationale) with and added EOF signal("stop pulse", figure 9, column 6, lines 5-14).

Consider claim 37, and as applied to claim 36 above, Rumbaugh, Bechtel et al., and Beiley et al. do not explicitly teach that a pulse width of the EOF signal is less than the pulse width of the LVAL signal.

However, Michael teaches that a pulse width of the EOF signal is less than the pulse width of the LVAL signal(The LVAL signal taught by Beiley et al. has to be wide enough to indicate the validity of an entire line of data which is composed of a large

number of bits. The EOF signal taught by Michael is only one bit long, as the signal of Michael comprises a start bit, eight data bits, and a stop bit(i.e. EOF signal, column 6, lines 18-30, see figure 9).

6. Claims 45 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bechtel et al.(U.S. Patent 5,990,469) in view of Rumbaugh.

Consider Claim 45, Bechtel et al. teach:

A method of communicating data between a camera and a remote host processor(column 23, line 46 through column 24, line 34), said method comprising the steps of:

providing a connection between a camera and a remote host processor, the cable connection including a power line for carrying power and a data signal line(Bechtel et al. teach that three pins are used for a serial interface(i.e. as a data signal line) between the microcontroller and the camera. Bechtel et al. also teach of a ground pin and a V+ supply pin(i.e. a pair of power wires). In column 23, line 46 through column 24, line 33, Bechtel et al. detail the serial peripheral interface (SPI) between the camera portion(ASIC XC4003E) and the processor(microcontroller(5)). Bechtel et al. teach that in the SPI there are three bi-directional lines for transmitting data and a slave select input (SS) which includes a ground(i.e. is a pair of power wires), the slave select input being operable to change the states of the camera and microcontroller alternately between master and slave.);

providing a trigger pulse from a host processor side link layer of the host processor to a camera side link layer of the camera through the power line(The slave select signal, which is provided by a pair of power wires as illustrated above, is driven to line low(i.e. provided a trigger pulse), which places the ASIC XC4003E(i.e. the camera side) in a slave state, column 24, lines 1-5.), wherein the trigger pulse is indicative of initiation of configuration of the camera(A nine byte instruction is transmitted following the trigger pulse, column 24, lines 5-6);

disabling data transmission from the camera side link layer and enabling a serial-to-camera (SERTC) channel receiver in the camera side link layer in response to receiving the trigger pulse on the power line(The camera is placed in slave mode(i.e. communication from the camera to the host processor is disabled), column 24, lines 1-6.);

monitoring the status of the signal line by examining outputs of the host processor side link layer(The readout of transmitted image data(i.e. the readout of the outputs of the signal lines) at the host processor is monitored by the microcontroller, which disables a reset function until the readout of the image data is completed, column 16, lines 11-14.);

enabling a SERTC channel transmitter located in the host processor side link layer to establish a serial communication interface (SCI) between the camera and the host processor via the signal line when the output indicates the signal line is free(The microcontroller(i.e. host processor) transmits(i.e. a transmitter is enabled) a reset function over the serial interface(i.e. a serial communication interface between the

camera coupled to the camera side and a host processor coupled to the host processor side) via the signal lines when the outputs indicate the signal lines are free(When the readout of the pixels is completed, the signal lines are free, and the microcontroller establishes SERTC communication with the camera and provides the "reset" instruction, column 15, line 52 through column 16, line 14, see also column 24, lines 13-33);

transmitting configuration data from the host processor to the camera(column 24, lines 1-6);

disabling the SERTC channel transmitter and the SERTC channel receiver and enabling the pixel data transmission in response to a reset message, wherein the reset message is provided by the host processor, and transmitting video data from the camera to the host processor via the signal line(See column 24, lines 1-25. The host processor sends a high slave select signal(i.e. a reset message), which places the camera in a master mode, the host processor in slave mode, and allows the transmission of pixel data from the camera to the host processor.).

However, Bechtel et al. do not explicitly teach that a serializer and deserializer are used, that a link layer is provided on the camera side and on the host processor side, or that the signal lines comprise a cable.

Rumbaugh is similar to Bechtel et al. in that a camera(100, figure 2) communicates with a host processor(112, figure 2) over a serial interface(Video data is transmitted serially over a twisted pair wiring(column 4, lines 1-9). Rumbaugh is also similar in that transmitter is disabled when not transmitting data(column 1, lines 18-35).

However, in addition to the teachings of Bechtel et al., Rumbaugh explicitly

teaches of the use of a serializer("Serial Interface", 101, figure 2) and a deserializer("serial interface buffer", 111, figure 2) in the transmission of video data(The camera side link layer converts the input signal into bits(i.e. a desired video data format) which are read into a serial interface, column 4, lines 31-33.). Rumbaugh also teaches that a link layer is provided on the camera side("Electronic Device Interface", 100, figure 2) and on the host processor side("Electronic Device Interface", 112, figure 2). The host processor link layer("digital data interface input device", 112, column 5, lines 34-36) can be used to connect to a computer(i.e. a host processor), column 5, lines 34-36. Rumbaugh further teaches that the signal lines comprise a cable(The cable is a twisted pair copper wire(i.e. a pair of power wires) for carrying power, column 4, lines 1-9.).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to include a serializer and a deserializer, camera side and host processor side link layers, and a cable between the camera and host processor as taught by Rumbaugh in the camera/host-processor serial interface taught by Bechtel et al. for the benefit that serializers and deserializers utilized in conjunction with camera side and host processor side link layers create a more versatile device since a multitude of different input and output devices with different configurations can utilize the transmission medium(Rumbaugh, column 4, lines 12-45), and a cable transmission allows more choices in the placement of the camera and host processor, while still maintaining high transmission rates, high quality of service, and a low bit error rate(Rumbaugh, column 1, line 50 through column 2, line 10).

Consider claim 46, and as applied to claim 45 above, Bechtel et al. teaches that the cable connection comprises a pair of power lines and a pair of data signal lines(A pair of power lines, including V+ and ground, are used to switch between master and slave settings(i.e. communicate configuration signals), column 23, line 46 through column 24, line 34. Bechtel et al. further teach at least a pair of data signal lines, as three bi-directional data signal lines are used, column 4, lines 39-44, column 23, lines 36-56.).

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert H. Cutler whose telephone number is (571)-270-1460. The examiner can normally be reached on Mon-Fri (7:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ngoc-Yen Vu can be reached on (571)-272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AC

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SUPERVISORY PATENT EXAMINER